A 100-GHz Monolithic Cascode InAlAs/InGaAs HEMT Oscillator

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***Abstract*— The design, fabrication,and experimental characteristics of a 100-GHz monolithic cascode HEMT oscillator are presented. A cascode pair of InAlAs/InGaAs HEMT's has been used as the active cell to enhance the negative resistance so that more process tolerance can be achieved. The monolithic circuit oscillates around 100 GHz with an output power of 2 dBm at a drain bias voltage as small as 0.9 V. This is the first demonstration of cascode HEMT oscillators at W-band.**

I. Introduction

INP-BASED HEMT's are recognized as the most suitable components for operation around 100 GHz and above due to their excellent high-frequency characteristics. Monolithic HEMT oscillators have been demonstrated at W-band using InAlAs/InGaAs HEMT's [1], as well as GaAs-based AlGaAs/InGaAs HEMT's [2]. Millimeter-wave oscillators present, in general, a rather small negative resistance at their output terminal due to limited gain of the transistor at these frequencies. Optimization of feedback topology can effectively increase the negative resistance at the desired frequency, as already shown by the authors for a D-band dual-feedback oscillator [3]. Another alternative to improve the negative resistance is to increase the gain by using a multi-transistor configuration. A cascode connected pair of transistors can be used for this purpose. This approach has the potential of high output resistance and good reverse isolation and is therefore suitable for high-frequency oscillator applications. Furthermore, the high negative resistance obtained in this way allows more precess tolerance as necessary for monolithic chips. The cascode configuration has been utilized in MMIC amplifiers for gain improvement up to W-band [4], [5]. In this work, cascode-connected HEMT's are employed to realize monolithic oscillators at 100 GHz.

II. Circuit Design and Fabrication

The oscillator design is based on a unit cell of cascode connected HEMT's. Two HEMT's are used for this purpose; the first one is in common source configuration and is followed by a second HEMT in common gate topology. The cascode pair offers higher output resistance and better reverse isolation, and thus less negative feedback compared with a single HEMT. It also exhibits higher power gain than the single HEMT. Its gain roll-off is, however, higher, resulting in the same f_T and f_{max}. The simulated maximum available gain (MAG) and reverse transmission (S_{12}) is compared in Fig. 1 for the single and cascode connected HEMT's and proves the advantage of the cascode HEMT pair. By way of an example, the cascode HEMT's used in this work provide about 8 dB more gain than individual HEMT's at 100 GHz when they are operated as an amplifier, and oscillators built with them show twice as much negative resistance. Oscillation conditions can consequently be better guaranteed, and larger latitude in terms of circuit design is achieved.

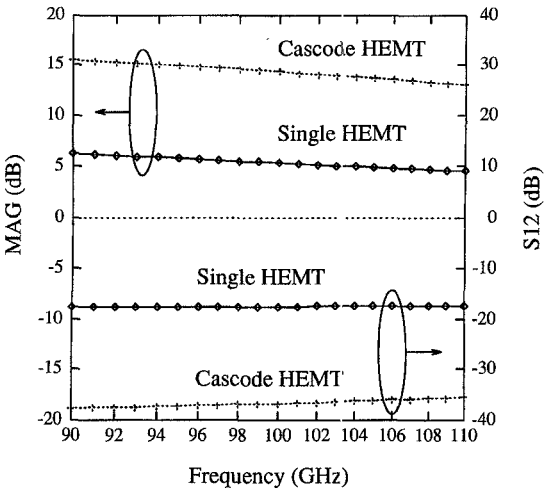

Fig. 1. Simulated maximum available gain (MAG) and reverse transmission (S_{12}) for single and cascode HEMT at frequencies around 100 GHz.

The equivalent circuit schematic of a 100-GHz monolithic cascode HEMT oscillator is shown in Fig. 2, together with the test fixture and measurement setup. The circuit employs common source configuration with a series source feedback realized with a narrow (20 μm) microstrip line. An output impedance transformer consisting of a single stub is used to provide the optimum load for maximum oscillation power at the drain terminal. The two HEMT's are DC decoupled using a dielectric overlay capacitor in order to provide independent bias control for each transistor. Bias was applied by on-chip networks consisting of a quarter-wavelength, high-impedance line and a radial stub. Circuit stability is improved by inte-

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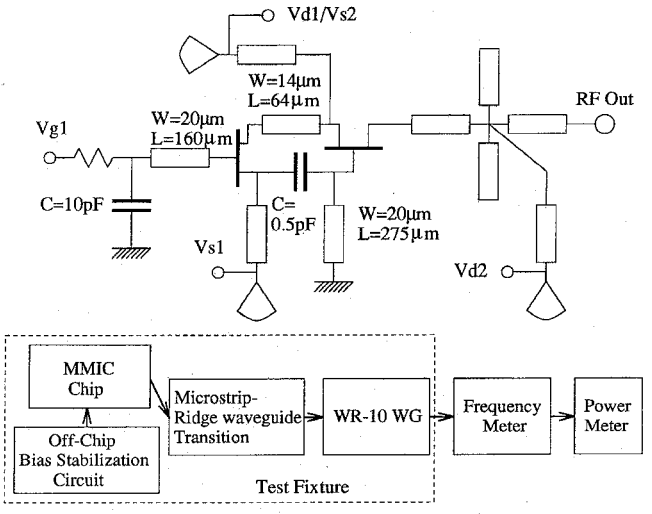

Fig. 2. Equivalent circuit schematic of 100-GHz monolithic cascode HEMT oscillator and measurement setup showing the schematic diagram of the test fixture.

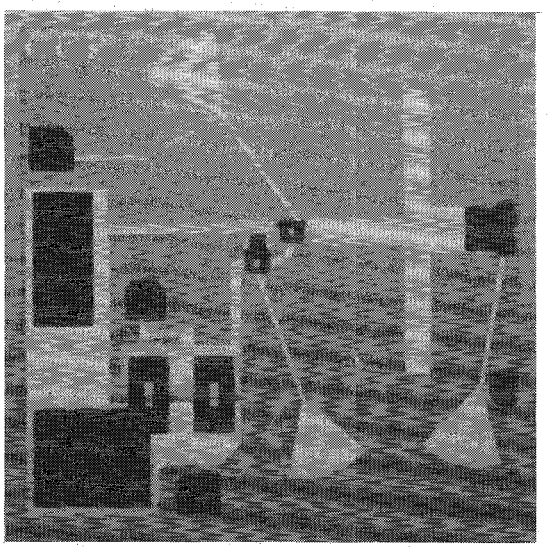

Fig. 3. Photograph of monolithic cascode HEMT oscillator. (Chip dimensions: 1 mm × 1 mm.)

grating in the gate bias line a 50 Ω resistor in addition to the off-chip bias stabilization circuit used for the mounted chips. This was designed to suppress undesired oscillations at lower frequencies and, in particular, at half the oscillation frequency (50 GHz). Microstrip lines used in the design had characteristic impedances in the range of 45 Ω to 95 Ω.

The HEMT layer design was based on the pseudomorphic double heterostructure (DH) approach and the wafer was grown by MBE at TRW. The details of the layer design and performance of DH-HEMT's compared with SH-HEMT's were presented previously by the authors in [6]. The device employs two InAlAs donor layers: one above and the other below the channel. The bottom donor layer helps to increase the carrier density in the channel and also provide additional carrier confinement, resulting in low output conductance. The DH design is very promising for oscillator applications since it provides a high current density and f_{max}. The monolithic oscillator was designed and fabricated at the University of Michigan using in-house-developed InP-based MMIC technology. E-beam lithography was used to define 0.1 μm T-gates, while optical lithography was used for the rest of the process steps. MIM capacitors were realized by lifting off sputtered SiO_2 and airbridges were formed by electroplating Au. The HEMT's used in the oscillator had two 45-μm-wide gate fingers. The DC transconductance was 800 mS/mm and the estimated MAG at 100 GHz was about 6 dB, yielding an extrapolated f_{max} value of 200 GHz, at the end of the MMIC process. A photograph of the 1 mm × 1 mm chip is shown in Fig. 3.

III. Measured Performance

The wafer was thinned to 100 μm and diced into individual chips for testing. The chips were mounted in a W-band test fixture with a ridge waveguide to microstrip transition. The test fixture showed a typical insertion loss of 1 dB over the whole W-band. The measurement results were corrected for 1 dB. Testing was done with the help of a power and a frequency meter. For testing, the gate biases were fixed at the value required for maximum transconductance and the drain biases were increased slowly. The chip broke into oscillation at a V_{ds} of 0.6 V and the oscillation frequency was 100.1 GHz, which is very close to the design frequency of 100 GHz. No external tuning was necessary for this operation. The dependence of the oscillation power on the drain bias is shown in Fig. 4. The output power is a strong function of V_{ds} and increased from -8.8 dBm to 2 dBm as V_{ds} is increased from 0.6 to 0.9 V. The corresponding DC-to-RF efficiency also increased from 1 % to 8 % with V_{ds}. These characteristics are limited by the low drain bias of 0.9 V currently employed due to the small drain-to-source breakdown voltage of the pseudomorphic $In_{0.7}Ga_{0.3}As$ channel design. Higher breakdown voltage and thus higher DC drain bias voltage would result in larger output power and higher efficiency. InP-based HEMT's combining a high aluminum percentage in the Schottky layer and modulation doping below, as well as above the channel showed the possibility of improving gate-drain breakdown voltage and increasing the current density [7]. Optimized structures of this type suggest the possibility of the high-gain InP-based cascode designs for millimeter-wave power application. The oscillation frequency dependence on V_{ds} is also shown in Fig. 4 and increased from 100.1 GHz at V_{ds}=0.6 V to 102.5 GHz at V_{ds}=0.9V. This behavior is likely to be due to the reduction of C_{gd} with V_{ds}.

IV. Conclusion

Oscillation at 100 GHz has been demonstrated for the first time by a cascode HEMT oscillator. The cascode design offers the possibility of providing higher gain and larger negative resistance that permit better process tolerance necessary for monolithic designs. This is also especially attractive for high-frequency applications, where the induced negative resistance of the single device is often quite small. Common source topology is employed for the oscillator circuit and DH In-

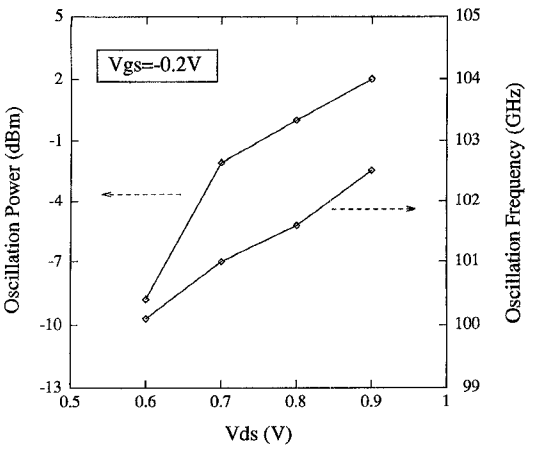

Fig. 4. Measured oscillation power and frequency dependence on the drain bias.

AlAs/InGaAs HEMT's were used as transistors. The oscillator chip was mounted on a test fixture with a ridge waveguide to microstrip transition for testing. The measured oscillation frequency (100.1–102.5 GHz) was very close to the design frequency (100 GHz), and an oscillation power of 2 dBm was obtained at a small drain bias of 0.9 V.

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